JC20 Rec'd PCT/PTO 05 APR 2002

Practitioner's Docket No. 57265 (45107)

CHAPTER II

TRANSMITTAL LETTER TO THE UNITED STATES ELECTED OFFICE (EO/US) (ENTRY INTO U.S. NATIONAL PHASE UNDER CHAPTER II)

PCT/EP00/09741	5 October 2000	06 October 1999
INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED

PROCESSOR SYSTEM, ESPECIALLY A PROCESSOR SYSTEM FOR COMMUNICATIONS DEVICES
TITLE OF INVENTION

Xiaoning NIE
APPLICANTS

Box PCT
Assistant Commissioner for Patents
Washington D.C. 20231
ATTENTION: EO/US

NOTE To avoid abandonment of the application, the applicant shall furnish to the USPTO, not later than 20 months from the priority date: (1) a copy of the international application, unless it has been previously communicated by the International Bureau or unless it was originally filed in the USPTO, and (2) the basic national fee (see 37 C.F.R. § 1 492(a)) The 30-month time limit may not be extended 37 C.F R § 1.495

WARNING: Where the items are those which can be submitted to complete the entry of the international application into the national phase are subsequent to 30 months from the priority date the application is still considered to be in the international state and if mailing procedures are utilized to obtain a date the express mail procedure of 37 C.F R §1 10 must be used (since international application papers are not covered by an ordinary certificate of mailing - See 37 C.F.R. §1.8.

NOTE: Documents and fees must be clearly identified as a submission to enter the national state under 35 USC 371 otherwise the submission will be considered as being made under 35 USC 111. 37 C F R § 1 494(f)

CERTIFICATION UNDER 37 C.F.R. § 1.10*
*(Express Mail label number is **mandatory.**)*
(Express Mail certification is optional)

I hereby certify that this paper, along with any document referred to, is being deposited with the United States Postal Service on this date April 5, 2002, in an envelope as "Express Mail Post Office to Addressee," mailing Label Number **EL932681287US**, addressed to the Assistant Commissioner for Patents, Washington, D C. 20231

Susan M Dillon
(type or print name of person mailing paper)

Susan M. Dillon
Signature of person mailing paper

WARNING: Certificate of mailing (first class) or facsimile transmission procedures of 37 C F.R § 1 8 cannot be used to obtain a date of mailing or transmission for this correspondence

WARNING: Each paper or fee filed by "Express Mail" **must have the number of the "Express Mail" mailing label placed thereon prior to mailing 37 C F R. § 1 10(b)*
*"Since the filing of correspondence under § 1.10 without the Express Mail mailing label thereon is an oversight that can be avoided by the exercise of reasonable care, requests for waiver of this requirement will **not** be granted on petition" Notice of Oct. 24, 1996, 60 Fed. Reg. 56,439, at 56,442.*

1. Applicant herewith submits to the United States Elected Office (EO/US) the following items under 35 U.S.C. 371:

   a. [X] This express request to immediately begin national examination procedures (35 U.S.C. 371(f)).

   b. [X] The U.S. National Fee (35 U.S.C. 371(c)(1)) and other fees (37 C.F.R. § 1.492) as indicated below:

2. Fees

CLAIMS FEE [ ]*	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS	14 - 20 =	0	x $ 18.00 =	$0
	INDEPENDENT CLAIMS	1 - 3 =	0	x $ 84.00 =	$0
	MULTIPLE DEPENDENT CLAIM(S) (if applicable) + $280.00				$280.00
BASIC FEE**	[ ] U.S. PTO WAS INTERNATIONAL PRELIMINARY EXAMINATION AUTHORITY Where an International preliminary examination fee as set forth in § 1.482 has been paid on the international application to the U.S. PTO: [ ] and the international preliminary examination report states that the criteria of novelty, inventive step (non-obviousness) and industrial activity, as defined in PCT Article 33(2) to (4) have been satisfied for all the claims presented in the application entering the national stage (37 CFR 1.492(a)(4)) ..... $100.00 [ ] and the above requirements are not met (37 CFR 1.492(a)(1)) ..... $710.00 [X] U.S. PTO WAS NOT INTERNATIONAL PRELIMINARY EXAMINATION AUTHORITY Where no international preliminary examination fee as set forth in § 1.482 has been paid to the USPTO, and payment of an international search fee as set forth in § 1.445(a)(2) to the U.S. PTO: [ ] has been paid (37 CFR 1.492(a)(2)) ..... $740.00 [ ] has not been paid (37 CFR 1.492(a)(3)) ..... $1040.00 [X] where a search report on the international application has been prepared by the European Patent Office or the Japanese Patent Office (37 CFR 1 492(a)(5)) $890.00				$890.00
				Total of above Calculations	= $1,170.00
SMALL ENTITY	Reduction by ½ for filing by small entity, if applicable. Affidavit must be filed. (note 37 CFR 1.9, 1.27, 1.28)				- $
				Subtotal	$1,170.00
				Total National Fee	$1,170.00
	Fee for recording the enclosed assignment document $40.00 (37 CFR 1.21(h)). (See Item 13 below). See attached "ASSIGNMENT COVER SHEET".				$0
TOTAL				Total Fees enclosed	$1,170 00

   i. [X] A check in the amount of $1,170.00 to cover the above fees is enclosed.

   ii. [ ] Please charge Account No. _____ in the amount of $ _____. A duplicate copy of this sheet is enclosed.

***WARNING* *"To avoid abandonment of the application the applicant shall furnish to the United States Patent and Trademark Office not later than the expiration of 30 months from the priority date· * * * (2) the basic national fee (see § 1.492(a)). The 30-month time limit may not be extended " 37 C F R § 1 495(b)*

WARNING *If the translation of the international application and/or the oath or declaration have not been submitted by the applicant within thirty (30) months from the priority date, such requirements may be met within a time period set by the Office 37 C.F R. § 1 495(b)(2). The payment of the surcharge set forth in § 1.492(e) is required as a condition for accepting the oath or declaration later than thirty (30) months after the priority date The payment of the processing fee set forth in § 1.492(f) is required for acceptance of an English translation later than thirty (30) months after the priority date. Failure to comply with these requirements will result in abandonment of the application. The provisions of § 1.136 apply to the period which is set. Notice of Jan. 3, 1993, 1147 O.G. 29 to 40.*

3. [X] A copy of the International application as filed (35 U.S.C. 371(c)(2)):

NOTE: *Section 1.495 (b) was amended to require that the basic national fee and a copy of the international application must be filed with the Office by 30 months from the priority date to avoid abandonment "The International Bureau normally provides the copy of the international application to the Office in accordance with PCT Article 20. At the same time, the International Bureau notifies applicant of the communication to the Office. In accordance with PCT Rule 47.1, that notice shall be accepted by all designated offices as conclusive evidence that the communication has duly taken place. Thus, if the applicant desires to enter the national stage, the applicant normally need only check to be sure the notice from the International Bureau has been received and then pay the basic national fee by 30 months from the priority date " Notice of Jan. 7, 1993, 1147 O G. 29 to 40, at 35-36. See item 14c below*

a. [ ] is transmitted herewith.
b. [ ] is not required, as the application was filed with the United States Receiving Office.
c. [X] has been transmitted
   i. [X] by the International Bureau.
   Date of mailing of the application (from form PCT/IB/308):
   ii. [ ] by applicant on _____.
   Date

4. [X] A translation of the International application into the English language (35 U.S.C. 371(c)(2)):
a. [X] is transmitted herewith.
b. [ ] is not required as the application was filed in English.
c. [ ] was previously transmitted by applicant on _____.
   Date
d. [ ] will follow.

5. [X] Amendments to the claims of the International application under PCT Article 19 (35 U.S.C. 371(c)(3)):

NOTE: *The Notice of January 7, 1993 points out that 37 C.F.R. § 1.495(a) was amended to clarify the existing and continuing practice that PCT Article 19 amendments must be submitted by 30 months from the priority date and this deadline may not be extended The Notice further advises that "The failure to do so will not result in loss of the subject matter of the PCT Article 19 amendments. Applicant may submit that subject matter in a preliminary amendment filed under section 1.121. In many cases, filing an amendment under section 1.121 is preferable since grammatical or idiomatic errors may be corrected." 1147 O.G 29-40, at 36.*

a. [ ] are transmitted herewith.
b. [ ] have been transmitted
   i. [ ] by the International Bureau.
   Date of mailing of the amendment (from form PCT/IB/308): _____.

ii. [ ] by applicant on _____.
Date

c. [X] have not been transmitted as
i. [X] applicant chose not to make amendments under PCT Article 19.
Date of mailing of Search Report (from form PCT/ISA/210): 19/03/01
ii. [ ] the time limit for the submission of amendments has not yet expired. The amendments or a statement that amendments have not been made will be transmitted before the expiration of the time limit under PCT Rule 46.1.

6. [X] A translation of the amendments to the claims under PCT Article 19 (38 U.S.C. 371(c)(3)):
a. [ ] is transmitted herewith.
b. [ ] is not required as the amendments were made in the English language.
c. [X] has not been transmitted for reasons indicated at point 5(c) above.

7. [X] A copy of the international examination report (PCT/IPEA/409)
[X] is transmitted herewith.
[ ] is not required as the application was filed with the United States Receiving Office.

8. [X] Annex(es) to the international preliminary examination report
a. [X] is/are transmitted herewith.
b. [ ] is/are not required as the application was filed with the United States Receiving Office.

9. [ ] A translation of the annexes to the international preliminary examination report
a. [ ] is transmitted herewith.
b. [ ] is not required as the annexes are in the English language.

10. [X] An oath or declaration of the inventor (35 U.S.C. 371(c)(4)) complying with 35 U.S.C. 115
a. [ ] was previously submitted by applicant on _____.
Date
b. [ ] is submitted herewith, and such oath or declaration
i. [ ] is attached to the application.
ii. [ ] identifies the application and any amendments under PCT Article 19 that were transmitted as stated in points 3(b) or 3(c) and 5(b); and states that they were reviewed by the inventor as required by 37 C.F.R. 1.70.
iii. [X] will follow.

Other document(s) or information included:

11. [X] An International Search Report (PCT/ISA/210) or Declaration under PCT Article 17(2)(a):
a. [X] is transmitted herewith.
b. [ ] has been transmitted by the International Bureau.
Date of mailing (from form PCT/IB/308): _____.
c. [ ] is not required, as the application was searched by the United States International Searching Authority.
d. [ ] will be transmitted promptly upon request.

e. [ ] has been submitted by applicant on _____.
Date

12. [X] An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98:
a. [X] is transmitted herewith.
Also transmitted herewith is/are:
[X] Form PTO-1449 (PTO/SB/08A and 08B).
[X] Copies of citations listed.
b. [ ] will be transmitted within THREE MONTHS of the date of submission of requirements under 35 U.S.C. 371(c).
c. [ ] was previously submitted by applicant on _____.
Date

13. [ ] An assignment document is transmitted herewith for recording.

A separate [ ] "COVER SHEET FOR ASSIGNMENT (DOCUMENT) ACCOMPANYING NEW PATENT APPLICATION" or [ ] FORM PTO 1595 is also attached.

_____
_____
_____

14. [X] Additional documents:
a. [X] Copy of request (PCT/RO/101)
b. [X] International Publication No. WO 01/25213
i. [X] Specification, claims and drawing
ii. [ ] Front page only
c. [X] Preliminary amendment (37 C.F.R. § 1.121)
d. [X] Other

Copy of amended claims under Article 34 and English translation
Form PCT/IB/304
_____

15. [X] The above checked items are being transmitted
a. [X] before 30 months from any claimed priority date.
b. [ ] after 30 months.

16. [ ] Certain requirements under 35 U.S.C. 371 were previously submitted by the applicant on _____, namely:

_____
_____

AUTHORIZATION TO CHARGE ADDITIONAL FEES

WARNING: *Accurately count claims, especially multiple dependent claims, to avoid unexpected high charges if extra claims are authorized.*

NOTE: *"A written request may be submitted in an application that is an authorization to treat any concurrent or future reply, requiring a petition for an extension of time under this paragraph for its timely submission, as*

incorporating a petition for extension of time for the appropriate length of time An authorization to charge all required fees, fees under § 1 17, or all required extension of time fees will be treated as a constructive petition for an extension of time in any concurrent or future reply requiring a petition for an extension of time under this paragraph for its timely submission Submission of the fee set forth in § 1 17(a) will also be treated as a constructive petition for an extension of time in any concurrent reply requiring a petition for an extension of time under this paragraph for its timely submission." 37 C F.R § 1 136(a)(3).

NOTE "Amounts of twenty-five dollars or less will not be returned unless specifically requested within a reasonable time, nor will the payer be notified of such amounts; amounts over twenty-five dollars may be returned by check or, if requested, by credit to a deposit account." 37 C F R. § 1.26(a).

[X] The Commissioner is hereby authorized to charge the following additional fees that may be required by this paper and during the entire pendency of this application to Account No. **04-1105**.

[X] 37 C.F.R. 1.492(a)(1), (2), (3), and (4) (filing fees)

WARNING: *Because failure to pay the national fee within 30 months without extension (37 C F R § 1 495(b)(2)) results in abandonment of the application, it would be best to always check the above box.*

[X] 37 C.F.R. 1.492(b), (c) and (d) (presentation of extra claims)

NOTE: Because additional fees for excess or multiple dependent claims not paid on filing or on later presentation must only be paid or these claims cancelled by amendment prior to the expiration of the time period set for response by the PTO in any notice of fee deficiency (37 C.F.R. § 1 492(d)), it might be best not to authorize the PTO to charge additional claim fees, except possible when dealing with amendments after final action.

[X] 37 C.F.R. 1.17 (application processing fees)

[X] 37 C.F.R. 1.17(a)(1)-(5)(extension fees pursuant to § 1.136(a).

[ ] 37 C.F.R. 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 C.F.R. 1.311(b))

NOTE Where an authorization to charge the issue fee to a deposit account has been filed before the mailing of a Notice of Allowance, the issue fee will be automatically charged to the deposit account at the time of mailing the notice of allowance 37 C.F R. § 1 311(b).

NOTE: 37 C.F.R. 1.28(b) requires "Notification of any change in loss of entitlement to small entity status must be filed in the application . . . prior to paying, or at the time of paying . . . issue fee " From the wording of 37 C F.R. § 1.28(b) (a) notification of change of status must be made even if the fee is paid as "other than a small entity" and (b) no notification is required if the change is to another small entity.

[ ] 37 C.F.R. § 1.492(e) and (f) (surcharge fees for filing the declaration and/or filing an English translation of an International Application later than 30 months after the priority date).

SIGNATURE OF PRACTITIONER

Reg. No.: 33,860

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(type or print name of practitioner)

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#129647

Docket No. 57265

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Xiaoning NIE

U.S.S.N.: Not Yet Assigned
[Express Mail Label No. EL931681287US]

FILED: Herewith

FOR: PROCESSOR SYSTEM, ESPECIALLY A PROCESSOR SYSTEM FOR COMMUNICATIONS DEVICES

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

PRELIMINARY AMENDMENT

Applicants kindly ask that the above-identified application be amended as follows:

IN THE CLAIMS:

Please cancel claims 1-12 without prejudice.

Kindly add the following new claims:

--13. Processor system, with a processor unit for executing instructions filed in a program memory, whereby the processor unit comprises instruction read out means for reading out an instruction from the program memory, and instruction decoding means for decoding the instruction and instruction executing means for executing the instruction,
whereby the instruction executing means comprise a plurality of executing units operable in parallel for parallel execution of various instructions, and the instruction read out means and the instruction decoding means (3) are jointly provided for all executing units, and wherein an executing unit of the instruction executing meansis connected to a first databus and a second executing unit is connected to a second databus whereby the transmission rate of the first databus is lower than the transmission rate of the second databus.

14. Processor system according to claim 13, wherein temporary storage means for storing information required for executing the instruction to be carried out by the particular executing unit are associated with each executing unit.

15. Processor system according to claim 13, wherein a first executing unit of the instruction executing means is designed to execute all instructions of a set of instructions of the processor system, and a second executing unit of the instruction executing means is designed to execute only a few special instructions of the instruction set.

16. Processor system according to claim 15, wherein the second executing unit is designed to execute only one special instruction of the instruction set of the processor system.

17. Processor system according to claim 16, wherein the second executing unit is designed to execute only an instruction to move a data block.

18. Processor system according to claim 14 wherein information stored in the temporary storage means associated with the second executing unit comprises a storage or loading address of the datablock to be stored or loaded, the amount of data elements of the datablock to be moved, an offset value, with which the datablock has to be stored or read and/or control information, which specifies whether the instruction to be carried out concerns a storage or read instruction.

19. Processor system according to claim 15 wherein the processor unit is designed in such a way that the path leading to the first executing unit is temporarily deactivated by the instruction read out means via the instruction decoding means, if momentarily no instruction has to be executed by the first executing unit.

20. Processor system according to claim 13 wherein the processor system is intended for processing telecommunications protocols, and the first databus is intended for processing header data of the telecommunications protocols, while the second databus is intended for fast transfer of payload data.

21. Processor system according to claim 13 wherein a data memory of the processor system is connected to the first databus, and at least one input and/or output port and/or at least one register or buffer is connected to the second databus.

22. Processor system according to claim 20 wherein the input and/or output port connected to the second databus is connected to a transmitter and/or receiver unit of a communication transmitter, and the register or buffer connected to the second databus is provided for temporary storage of a bitstream to be transmitted or received by the communication transmitter.

23. Processor system according to claim 15, wherein the executing unit of the instruction executing means connected to the first databus corresponds to the first executing unit and the executing unit connected to the second databus corresponds to the second executing unit.

24. Processor system according to claim 23 wherein the first executing unit is also connected to the second databus, so that it can also access the second databus, while the second executing unit is only connected to the second databus.

REMARKS

Claims 13-20 have been added and 1-12 have been cancelled without prejudice. No new matter is presented by virtue of this amendment. For instance, support for claims 13-20 appears e.g. in the original claims.

Applicants respectfully request entry of this Amendment prior to examination.

Early consideration and allowance of the application are earnestly solicited.

Respectfully submitted,

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2/pr15

Description

Processor system, especially a processor system for communications devices

Communications controllers are used in communication transmitters, routers or gateways, which for the sake of simplicity are described below as host systems. Normally receiving and transmitting communication information is managed or controlled with the aid of the communications controllers. For transmission the communication information present in the form of digital data is collected from a buffer and subsequently, possibly packaged with further information bits, written to a transmission buffer. The content of the transmission buffer is subsequently forwarded to a modulator or transceiver, which modulates the digital transmission data onto a carrier signal, converts it from digital to analogue and tranmits it via a communications channel to a receiver.

The communication information is processed in agreement with so-called communications protocols, which are structured in the form of layers, individually described as "layer". In the transmitting direction the input data of the particular layer must be packaged with a so-called protocol header in each layer and forwarded to the subordinate layer. In the receiving direction on the other hand the particular input data must be extracted from the protocol header and the data must be forwarded to the superior layer in each case. Therefore as well as evaluating and executing control instructions for example externally fed via a host computer or microcontroller the main objectives of a communications controller are to extract the header information from an incoming bitstream, to insert the header information in a bitstream to be

transmitted and to forward the particular data to another layer (i.e. the data transfer).

With regard to the architecture of communications controllers various proposals are known, which essentially can be characterised by the central processor unit (CPU), the memory structure, the bus structure or the instruction set used in each case. Typical communications controller architecture is described for example in "A 16Mb/s Adapter Chip for the IBM Token-Ring Local Area Network", J. D. Blair et. al., IEEE Journal of Solid-State Circuits, vol. 24, December 1989. The data transfer detailed above often represents a bottleneck in the communications controller. In the case of the known architecture previously mentioned this results in the changeover from one program sequence to another program sequence, also described as "task switch", taking a relatively long time.

For this reason communications controllers have been proposed, the architecture of which enables various instructions or program sequences to be processed in parallel. Thus for example in the US patent 5,434,976 a communications controller is proposed, which has two central processor units (CPU's) independent of each other, each processor unit possessing its own path for collecting or reading out an instruction to be executed and for decoding and executing the read out instruction. Essentially the function of the so-called MAC-layer ("Medium Access Control") is performed with the aid of one of the processor units while the other processor unit essentially executes host instructions and handles the buffer memory functions associated with receiving or transmitting data.

Although it is possible with the aid of this known architecture to efficiently process the communication information, especially to transfer data relatively quickly, this architecture has the disadvantage that two separate processor units are required, which increases the necessary chip space as well as the power consumption.

The object of the present invention is therefore based on proposing a processor system, which on the one hand has minimal chip space requirement and power consumption and on the other hand makes it possible for the functions needed for processing communication information to be executed quickly and efficiently.

This object is achieved according to the invention by a processor system with the features of claim 1. The sub-claims define preferred and advantageous embodiments of the present invention.

The processor system according to the invention in particular designed in the form of a communications controller only has one central processor unit (CPU) to execute instructions stored in a program memory, the processor unit having a single path for reading out an instruction from the program memory and for decoding the read out instruction. In addition several execution paths operable in parallel are provided for parallel execution of various instructions or program sequences, which each access the path used jointly for reading out and decoding an instruction.

In this way the parallel processing of different program sequences is possible in principle, whereby the chip space requirement and power consumption can be minimised owing to

the path being used jointly for reading out and decoding the instructions.

It is advantageous if only one of the execution paths performs the normal computing and addressing functions of the CPU while another execution path only carries out certain special functions, so that this execution path can be implemented more simply and the complexity of design can be further reduced. It is particularly advantageous if the latter execution path can only execute one particular frequently required function, whereby during the processing of communications protocols this can for example be the movement of data blocks, i.e. the data transfer.

To move, i.e. load or store, data blocks the instruction set of the processor system can be advantageously expanded in such a way that with the corresponding "block move" instruction a programmable offset value is pre-set at the same time, as the result of which the data block for example is written to an output port or read out from an input port. In this case in particular a bitoffset can be used as offset value.

By using databuses with different transmission rates less frequently required or slower functions can be executed on the databus at the lower transmission rate, while functions which are required more frequently or those to be executed quickly, as for example in particular data transfers, can be executed via the databus at the higher transmission rate. This embodiment according to the invention is therefore different from the known solutions, which either propose the use of an individual databus in combination with a single processor unit or the use of two separate databuses in combination with two separate processor units.

In the case of a communications controller of the so-called payload data can be quickly transferred in this way on the databus provided with sufficient bandwidth, having the higher transmission rate, while the protocol-header data is processed by the slower databus.

Further advantages of the present invention, which result from the previously described architecture of the processor system according to the invention, are amongst others the use of different bitwidths for the individual databuses and a heterogeneous memory hierarchy for the ports, registers and RAM-data memory of the processor system as well as the possibility of implementing different energy saving modes for each execution path and each databus.

The present invention is explained in more detail below with reference to the attached drawing by way of preferred embodiments.

Fig. 1 shows a simplified block diagram of a central processor unit or central unit (CPU) according to one embodiment of the present invention,

Fig. 2 shows the use of the processor unit shown in Fig. 1 with a processor system according to the invention, and

Figs. 3A-3C show enlarged illustrations of the input/output ports and registers illustrated in Fig. 2.

As shown in Fig. 1, the processor unit 1 (CPU) serving as communications controller for example of a communication transmitter includes a path for reading out and decoding an instruction from a program memory 8 of the

processor system, which is illustrated in Fig. 1 in the form of function blocks 2 and 3.

In order to optimise the data transfer to be executed during the processing of communication data as well as the protocols, instructions can be executed in parallel, parallelity only being present after the function blocks 2 and 3 and as the result of several executing units 5, 7 operable in parallel. Especially in the case of the embodiment shown in Fig. 1 two such parallel executing units 5, 7 are provided for independently processing various instructions or program sequences, a buffer memory or register 4 or 6 being associated with each executing unit after the decoding step 3. These buffer memories 4, 6 in each case serve to store information, which the following executing unit 5 or 7 requires to carry out the instructions.

According to the architecture shown in Fig. 1 therefore only a single path 2, 3 which is used jointly by all executing units 5, 7 operable in parallel, is required for collecting or reading out and decoding an instruction, resulting in more simple implementation and programming.

The executing units 5 and 7 are advantageously designed or structured differently. One of these executing units should be structured as simply as possible to reduce the complexity of design, so that only a limited number of functions or instructions can be executed, while at least one other executing unit can be kept as general as desired and in particular able to execute all possible functions or instructions. In the case of the embodiment illustrated the executing unit 7 is even simplified to such an extent that it is only designed to execute one particular instruction, preferably the instruction to move a datablock, while the

executing unit 5 can execute the entire instruction set of the processor system. In this way the structure of the bufffer 6 and the executing unit 7 can be simplified in comparison to the structure of the buffer 4 and the executing unit 5.

As already mentioned the buffers 4 and 6 each serve to temporarily store information, which is needed for executing the instruction to be carried out in the particular execution path. When instructions which last several cycles are executed (as for example in the case of a data block movement instruction), the information needed in each case is stored in the buffers 4 or 6 in order in this way to make the path with the function blocks 2 and 3 free for parallel execution of another instruction. If the executing unit 7 only serves to execute the instruction to move a datablock, only a bit to differentiate between a loading and a storage instruction, the address of the data source or data sink, the number of the data elements to be moved (for example bytes) as well as possible subsequent offset information, explained in detail below (for example bit offset information), must be stored in the corresponding buffer 6.

If the executing unit 7 is active for executing a data transfer, the execution path of the executing unit 5 can be accessed in parallel with a further program sequence ("task"). Its own state variables, which form the structural space of the particular program sequence also described as "context", are associated with each program sequence. Separate hardware, such as for example program counters and registers to store the particular state variables (zero bits, carry bits, address pointers etc.) should be provided for each active program sequence, so that when one program sequence is changed over to another

the hardware present in each case is switched over with the corresponding state variables and the context can be changed over without loss of cycle.

For so-called multitasking or parallel operation a set of instructions is necessary which amongst others includes instructions for starting and stopping a program sequence, giving specific priority to a program sequence or waiting for a signal concerning program sequence synchronisation. If the executing unit 5 has no further instructions to execute, it is intended that the entire path from function block 2 as far as function block 5 as well as the corresponding register for the state variables can be switched off, which likewise can result from an explicit instruction for switching off the clock.

Since each of the two executing units 5, 7 are associated with different program sequences, communication between the ALU ("Algorithmic Logical Unit"), the registers, RAM-memories and databus etc. of the processor system is simplified. Since the data of a program sequence in the executing unit 7 can be transferred in parallel to another program sequence, which is processed by the executing unit 5, in contrast to a DMA-based processor system ("Direct Memory Access"), better control can also be achieved within the software if the data movement instruction has had to be interrupted. In addition no management of DMA controllers is required, which contributes to reducing the program code and power requirement. Also hardware costs are minimised, since the registers or buffers 4, 6 can be used several times and no extra registers are necessary for the DMA-controllers.

As already mentioned, preferably the executing unit 7 only serves to execute a datablock movement instruction, while

the executing unit 5 can be designed as generally as possible, so that all possible functions or instructions can be executed. During processing of communication data the executing unit 7 can therefore be used for executing data transfers, while the executing unit 5 in parallel with this performs the rest of the protocol processing. Since the data transfers must be run relatively quickly in comparison to protocol processing, it is advantageous to connect the executing unit 7 to a databus with a relatively high transmission rate. This should be become clearer by referring to Fig. 2.

The central processor unit 1 is connected inside the processor system to two databuses 9 and 10, the databus 9 having a higher transmission rate than the databus 10. The processor unit 1 can only access the databus 9 with its executing unit 7, while the executing unit 5 which is designed in general can use both databuses 5, 7. To implement fast data transfers, especially to move the so-called payload data of communications protocols, which comprise the actual communication information, input- and output ports 11 as well as buffers or registers 12 are connected to the fast databus 9. The ports 11 are designed as more complex special registers and serve as the interface to a transceiver 14, also described as a modulator, of the corresponding communication transmitter, via which data is transmitted or received. An interrupt controller 16 in particular evaluates interrupt signals generated by the ports 11 and, depending on this in agreement with a preset interrupt handling, actuates the central processor unit 1. The buffers 12 form the interface to the particular host system 15 (i.e. the particular communication transmitter, router or gateway), which writes to or reads out from the buffer 12 the bitstream to be transmitted or received. The buffers 12 for example

designed as RAM memories can be controlled via DMA controllers configurable by the processor unit 1 so that the data transfers between the buffers 12 and the host system 15 puts no significant burden on the processor unit 1. The slower databus 10 on the other hand is linked with the actual data memory 13 of the processor system, which is designed in the form of a RAM mass memory and preferably serves to temporarily store the control data and header information of a communications protocol.

In this way the components 11, 12 provided for processing communications protocols to transfer so-called payload data are separated from the section provided for processing the protocol-header data, and the executing unit 7 as well as the fast databus 9 are used so that the payload data can be transferred quickly, while the header data of the particular communications protocol can be processed via the slower databus 10 (and the executing unit 5) in parallel with this.

The signals fed to a port 11 with serial data input and parallel data output are represented in Fig. 3A. This port 11 receives serial input data D_IN, which is written to the port 11 according to a clock signal CLK. In addition the port 11 receives 3 bit control information BP, which describes the bit position of the data to be written, as well as further 3 bit control information BW, which describes the width or length of the bit field to be written. In this way a data block of the length BW with a bitoffset of the length BP related to the first bit position of the port 11 is written to the port 11. As a further control signal a reset signal RESET is fed to the port 11. On the output side the data with n bits is read out in parallel, reading out of the data being released via a further control signal D_READ. Furthermore an interrupt

signal D_READY is provided, which produces an interrupt, if data is stored in the port 11.

The signals fed to a port 11 with parallel data input and serial data output are shown in Fig. 3B, this port only being distinguished from the port shown in Fig. 3A in that on the input side n-bits are read in in parallel and the output data is output in series.

Finally the signals fed to a buffer or register 12 are also shown in Fig. 3C, data elements in the form of bytes preferably being written to and read out from the buffer 12. In addition an address signal ADR is defined, which in each case describes the address of the buffer 12, which has to be accessed.

New claims

1. Processor system, with a processor unit (1) for executing instructions filed in a program memory (8), whereby the processor unit (1) comprises instruction read out means (2) for reading out an instruction from the program memory (8), and instruction decoding means (3) for decoding the instruction and instruction executing means (4-7) for executing the instruction, whereby the instruction executing means (4-7) comprise a plurality of executing units (5,7) operable in parallel for parallel execution of various instructions, and the instruction read out means and the instruction decoding means (3) are jointly provided for all executing units (5,7), **characterised in that** an executing unit (5) of the instruction executing means (4-7) is connected to a first databus (10) and a second executing unit (7) is connected to a second databus (9) whereby the transmission rate of the first databus (10) is lower than the transmission rate of the second databus (9).

2. Processor system according to claim 1, **characterised in that** temporary storage means (4,6) for storing information required for executing the instruction to be carried out by the particular executing unit (5,7) are associated with each executing unit (5,7).

3. Processor system according to claim 1 or 2, **characterised in that** a first executing unit (5) of the instruction executing means (4-7) is designed to execute all instructions of a set of instructions of the processor system, **and in that** a second executing unit (7) of the instruction executing means (4-7) is designed to execute only a few special instructions of the instruction set.

4. Processor system according to claim 3, **characterised in that** the second executing unit (7) is designed to execute only one special instruction of the instruction set of the processor system.

5. Processor system according to claim 4, **characterised in that** the second executing unit (7) is designed to execute only an instruction to move a data block.

6. Processor system according to claim 5 and claim 2, **characterised in that** the information stored in the temporary storage means (6) associated with the second executing unit (7) comprises a storage or loading address of the datablock to be stored or loaded, the amount of data elements of the datablock to be moved, an offset value, with which the datablock has to be stored or read and/or control information, which specifies whether the instruction to be carried out concerns a storage or read instruction.

7. Processor system according to one of claims 3-6, **characterised in that** the processor unit (1) is designed in such a way that the path leading to the first executing unit (5) is temporarily deactivated by the instruction read out means (2) via the instruction decoding means (3), if momentarily no instruction has to be executed by the first executing unit (5).

8. Processor system according to one of the previous claims, **characterised in that** the processor system (8) is intended for processing telecommunications protocols, **and in that** the first databus (10) is intended for processing header data of the telecommunications

protocols, while the second databus (11) is intended for fast transfer of payload data.

9. Processor system according to one of the previous claims, **characterised in that** a data memory (13) of the processor system is connected to the first databus (10), **and in that** at least one input and/or output port (11) and/or at least one register or buffer (12) is connected to the second databus (9).

10. Processor system according to claim 8 and 9, **characterised in that** the input and/or output port connected to the second databus (9) is connected to a transmitter and/or receiver unit (14) of a communication transmitter, **and in that** the register or buffer (12) connected to the second databus (9) is provided for temporary storage of a bitstream to be transmitted or received by the communication transmitter.

11. Processor system according to one of the above claims and one of claims 3-7, **characterised in that** the executing unit of the instruction executing means (4-7) connected to the first databus (10) corresponds to the first executing unit (5) and the executing unit connected to the second databus (9) corresponds to the second executing unit (7)

12. Processor system according to claim 11, **characterised in that** the first executing unit (5) is also connected to the second databus (9), so that it can also access the second databus (9), while the second executing unit (7) is only connected to the second databus (9).

Abstract

Processor System, especially a processor system for communications devices

The invention relates to a processor system which is configured as a communications controller and which comprises a central processor unit (1) for executing instructions filed in a program memory (8), whereby the processor unit (1) comprises only one path (2,3) for reading out an instruction from the program memory (8) and for decoding the instruction. In addition, several parallelly operable execution paths (4,5;6,7) for parallelly executing different program flows are provided which each access the path (2,3) jointly used for reading out and decoding an instruction.

(Fig. 1)

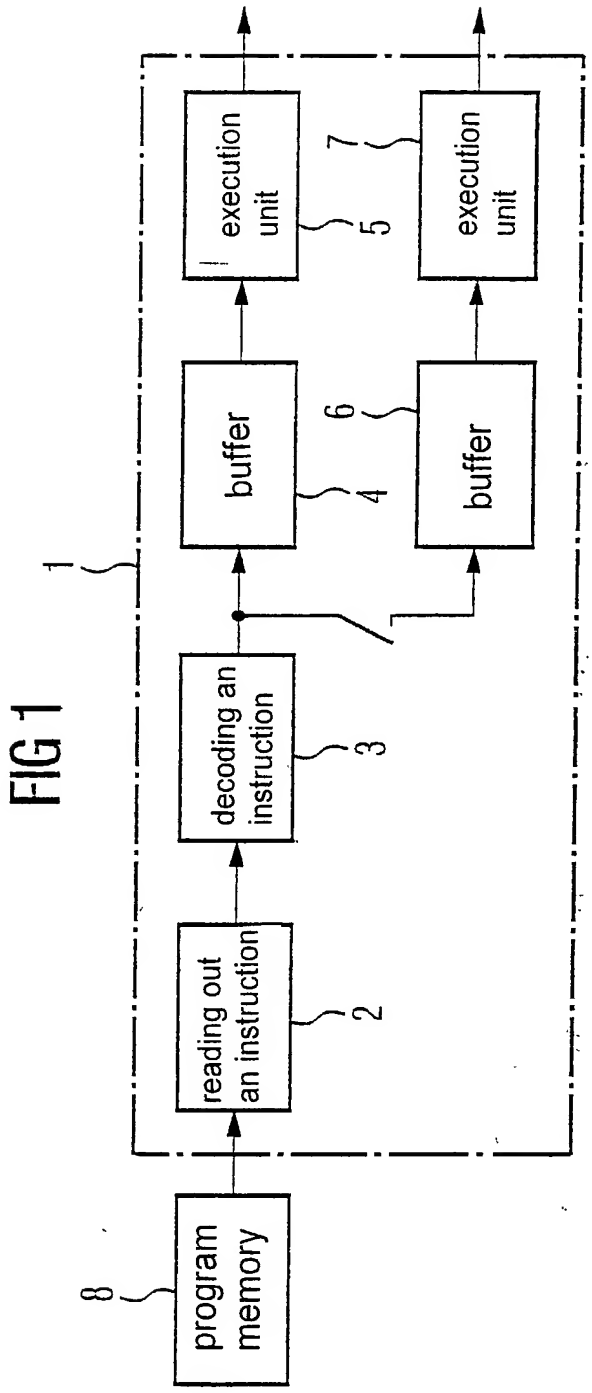

program memory
8
reading out an instruction
2
decoding an instruction
3
buffer
4
buffer
6
execution unit
5
execution unit
7
1

FIG 1

FIG 2

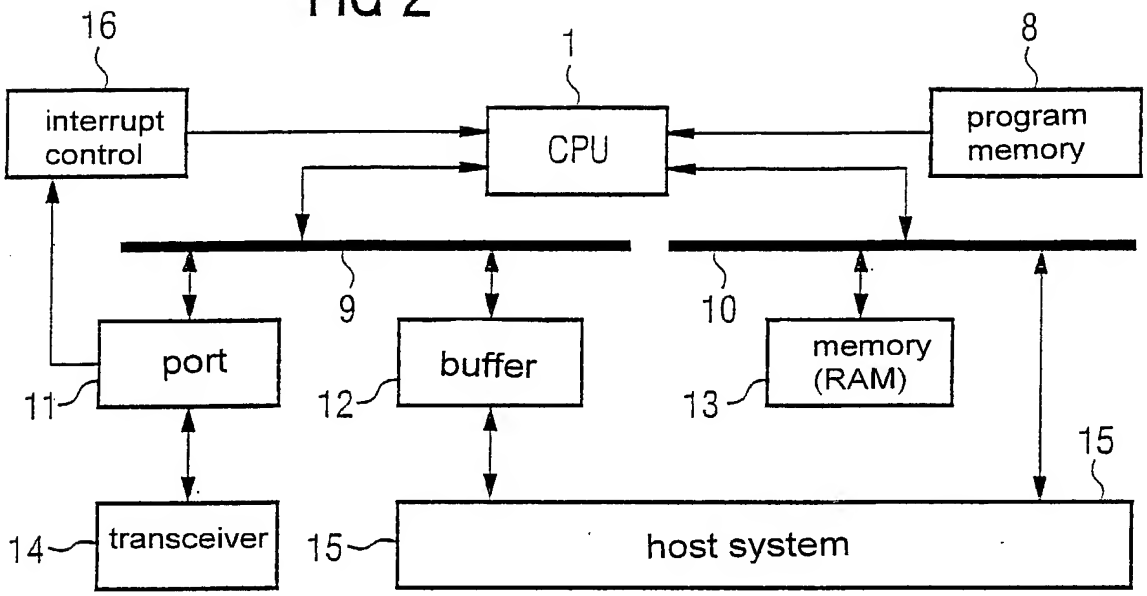


FIG 3A

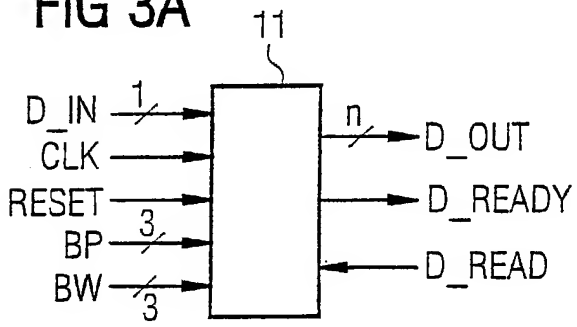


FIG 3B

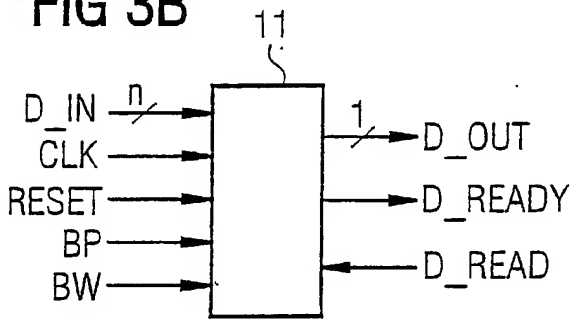
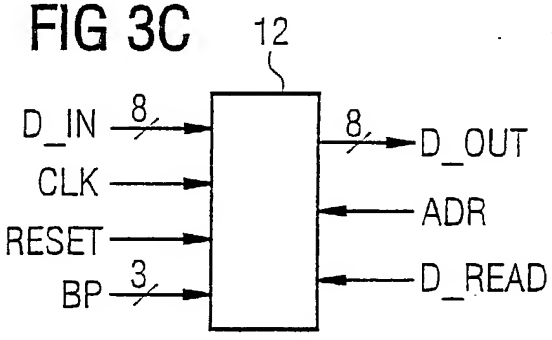


FIG 3C



#4

Express Mail Label No.

Docket No. 57265 (45107)

Declaration and Power of Attorney for Patent Application
English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

"PROCESSOR SYSTEM, ESPECIALLY A PROCESSOR SYSTEM FOR COMMUNICATION DEVICES "

the specification of which

(check one)

[ ] is attached hereto.
[X] was filed on 5 October 2000 as United States Application No. or PCT Application No. PCT/EP00/09741
and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
199 48 099.0 (Number)	Germany (Country)	6 October 1999 (Day/Month/Year Filed)	[ ]
(Number)	(Country)	(Day/Month/Year Filed)	[ ]
(Number)	(Country)	(Day/Month/Year Filed)	[ ]

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U.S.C. Section 120 of the United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark office all information known to me to be material to patentability as defined in Title 37, C.F.C., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
PCT/EP00/09741	5 October 2000	Pending
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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